Silicon nanowires for thermoelectric harvesting applications: growth, integration and characterization

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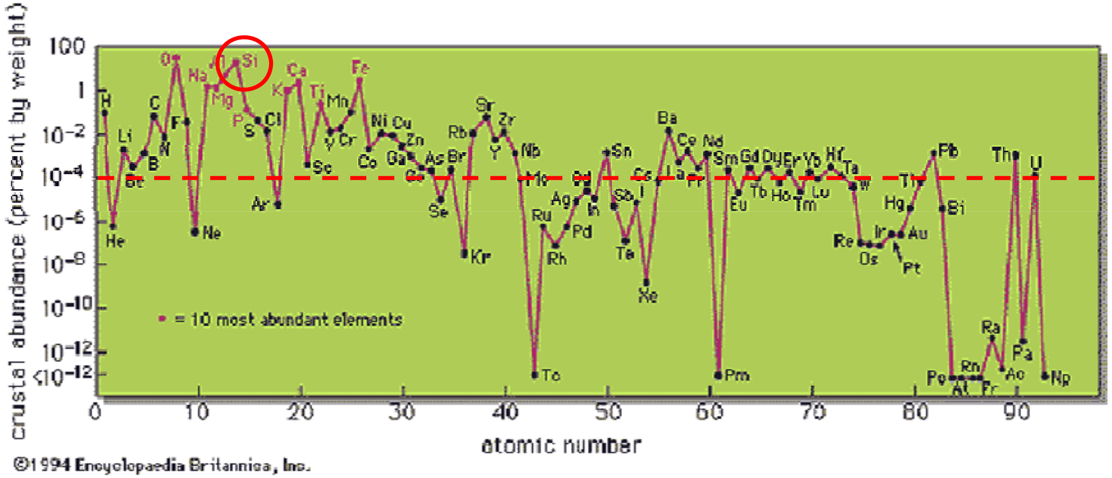
Lille, EMRS May 2016

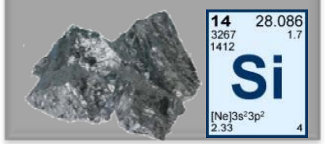
Thermoelectric energy harvesting with silicon nanowires

Si NWs are promising materials TE energy harvesting because:

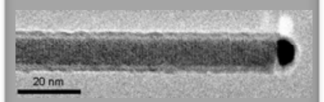
- Their high ZT with respect bulk
- The high availability of silicon
- The easy integrability in micro-technology (which is silicon-based!)

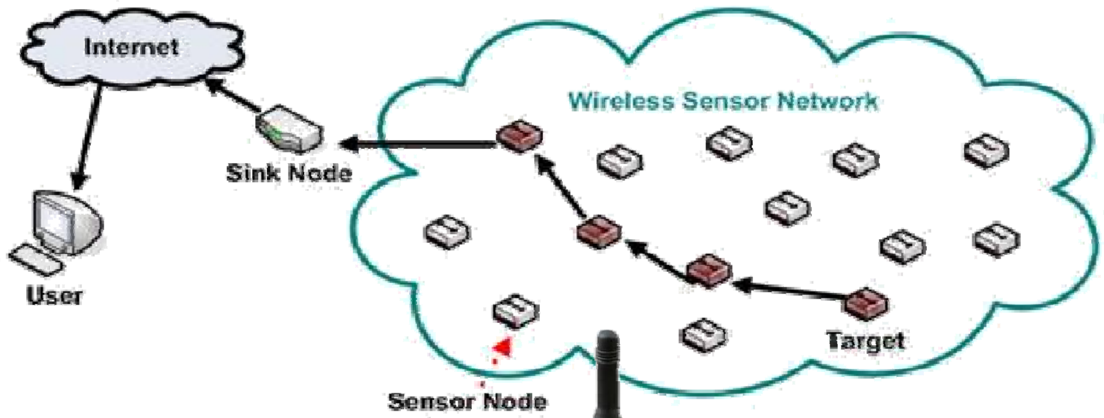


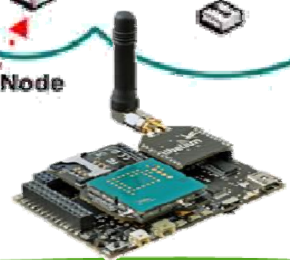
Doped Si: ZT=0.02 @ RT



Si NWs: ZT=0.60 @ RT







P needed: ~ µ10 W/cm²

WSN node

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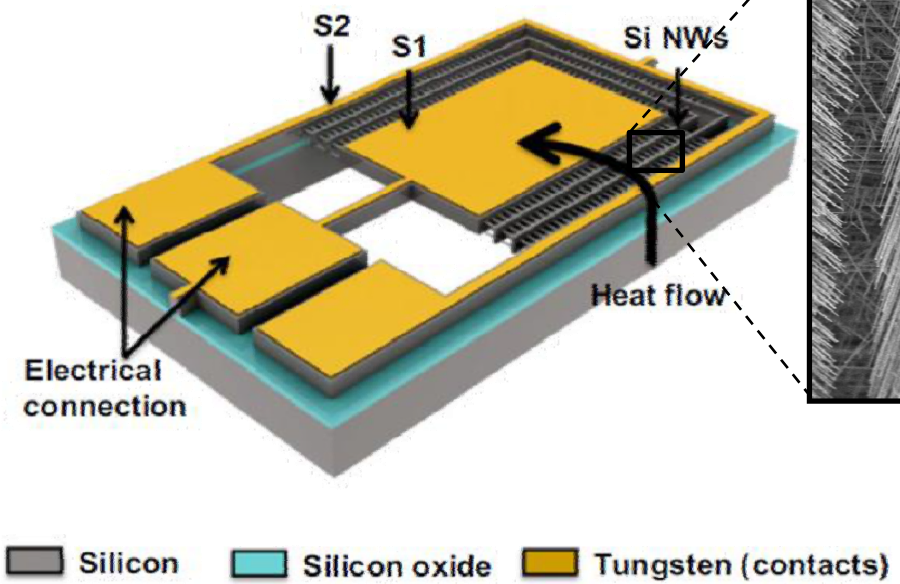
Thermoelectric energy harvesting with silicon nanowires

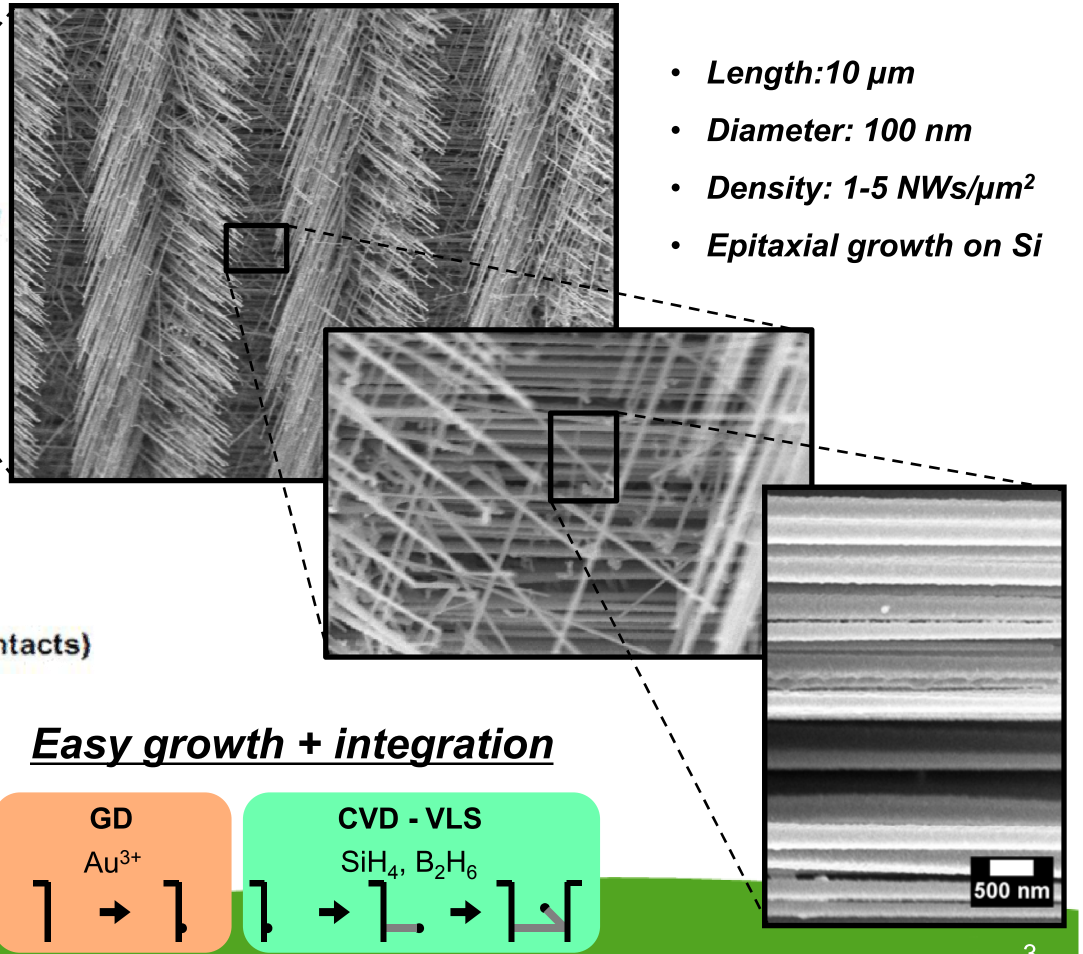
Integrating NWs in thermoelectric devices presents challenges:

- Contacting dense arrays of NWs / cm^2
- NWs with low contact resistance
- Submitting NWs to large ΔT
- Using technology friendly techniques

For this we use a micro-machined **planar thermoelectric generator (μTEG)**



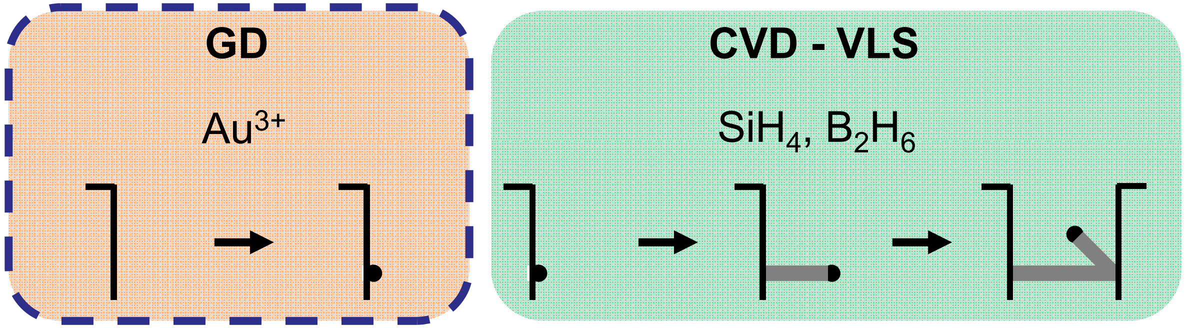
From D. Dávila et al. ***Nano Energy***, *1*(6), (2012) 812

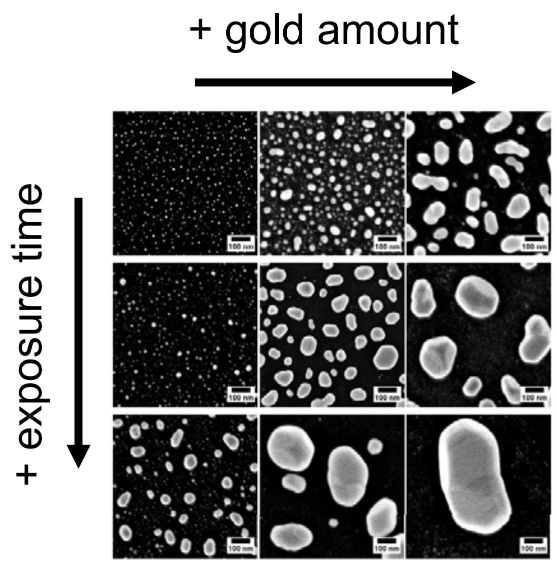


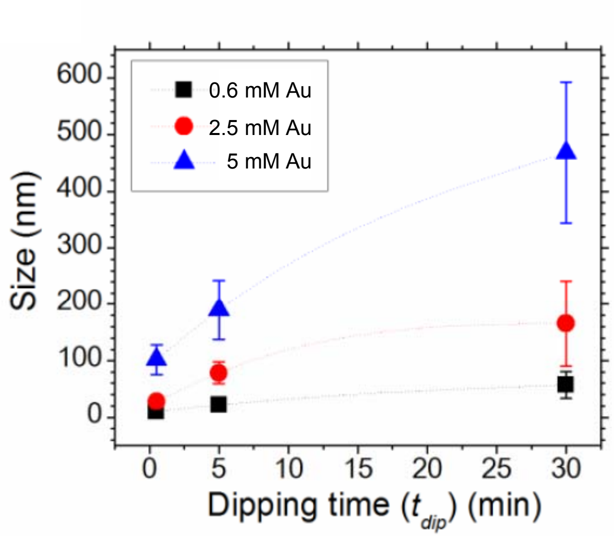
- ***Length:10 μm***
- ***Diameter: 100 nm***
- ***Density: 1-5 NWs/μm^2***
- ***Epitaxial growth on Si***

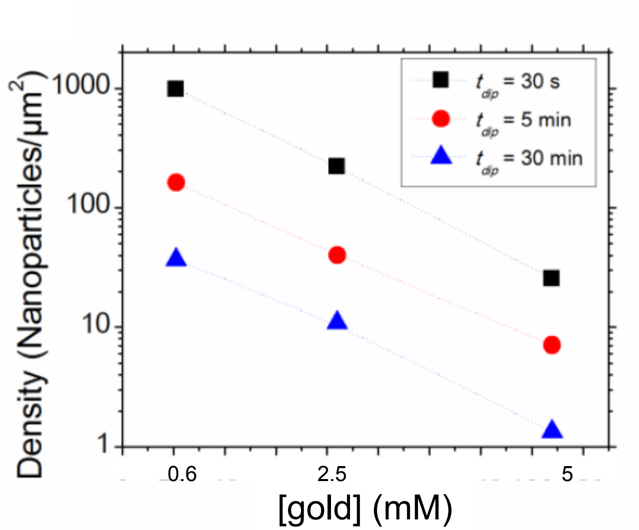
Easy growth + integration

Silicon nanowire morphology control





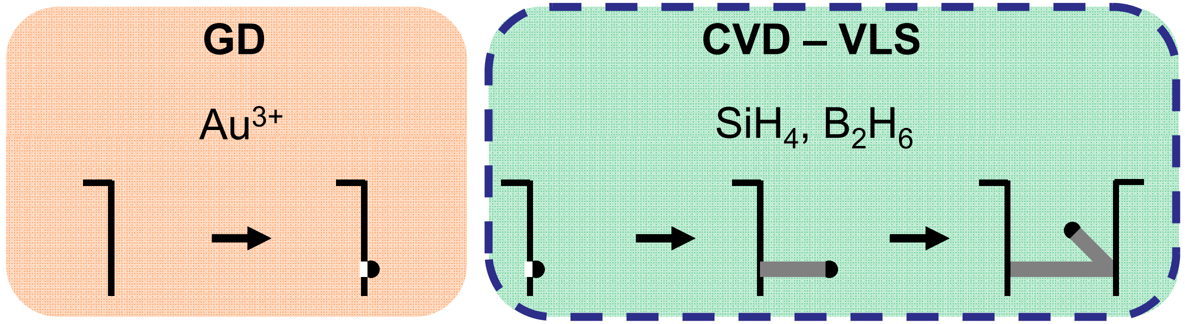




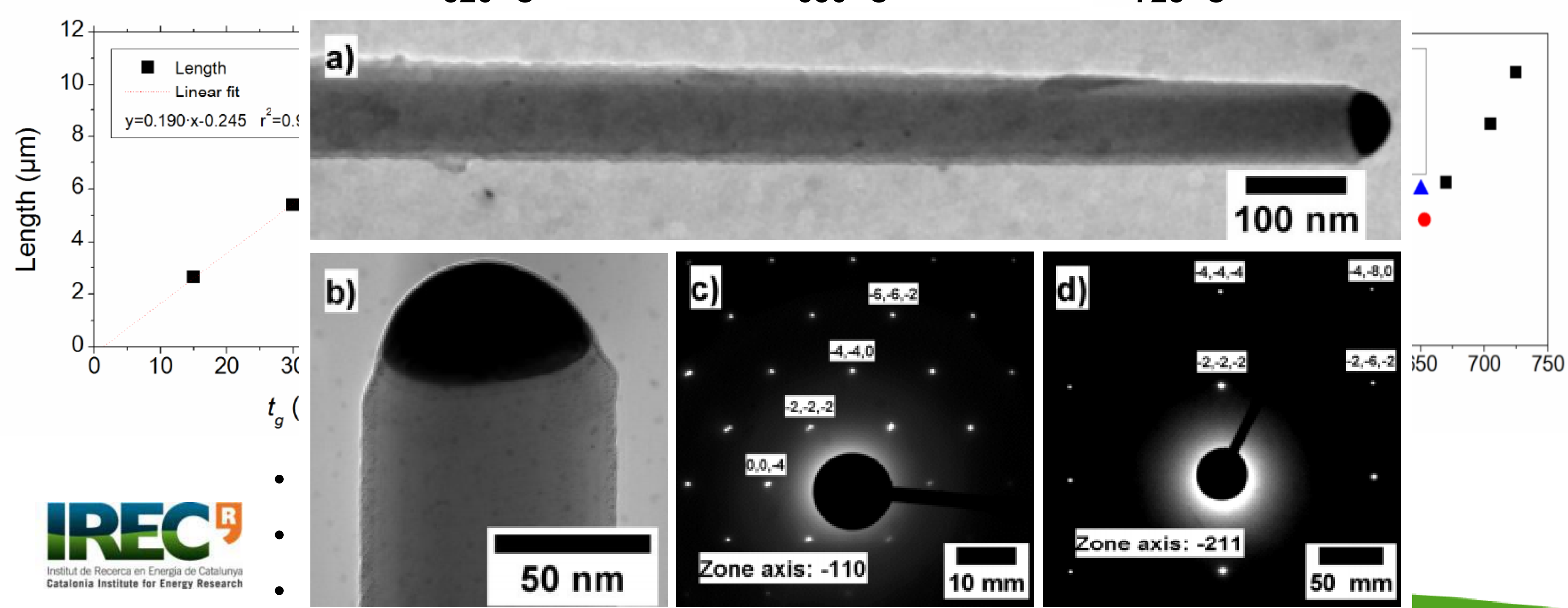
- Increasing the gold amount/exposure time, the nanoparticle size increases and while the density decreases

*From G. Gadea et al., **Nanotechnology**, 26 (2015) 195302*

Silicon nanowire morphology control

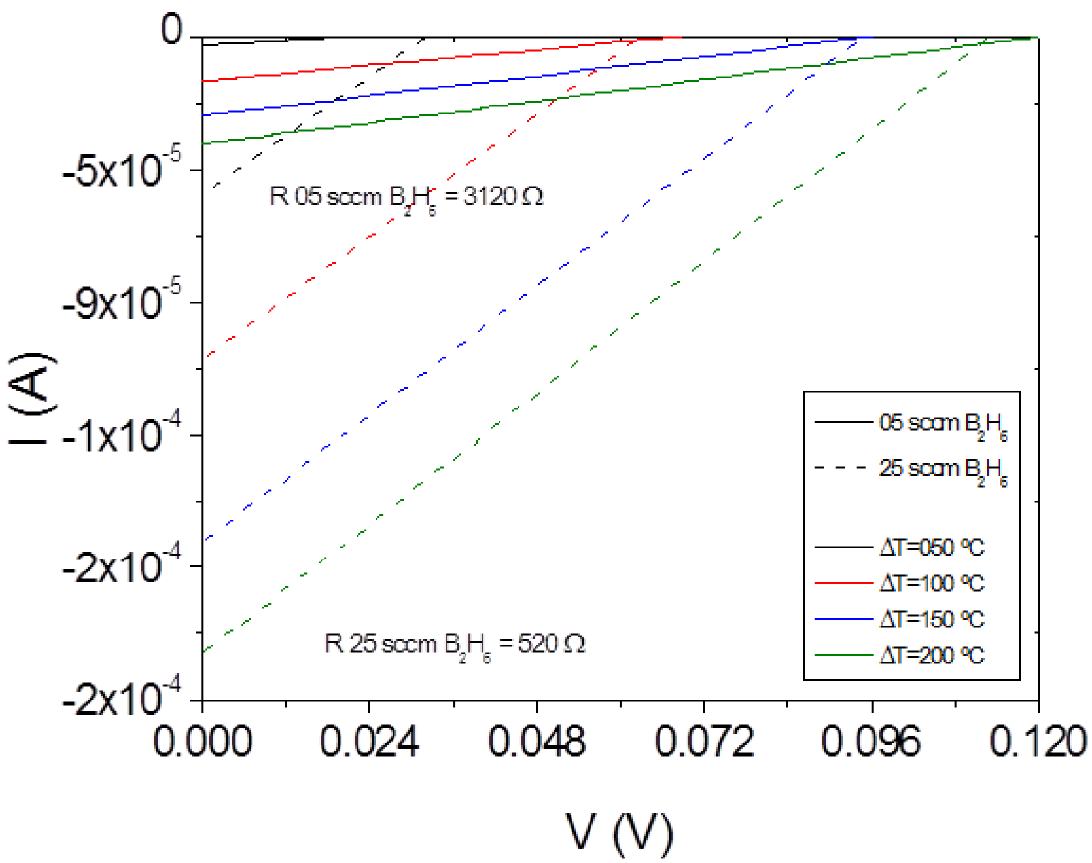


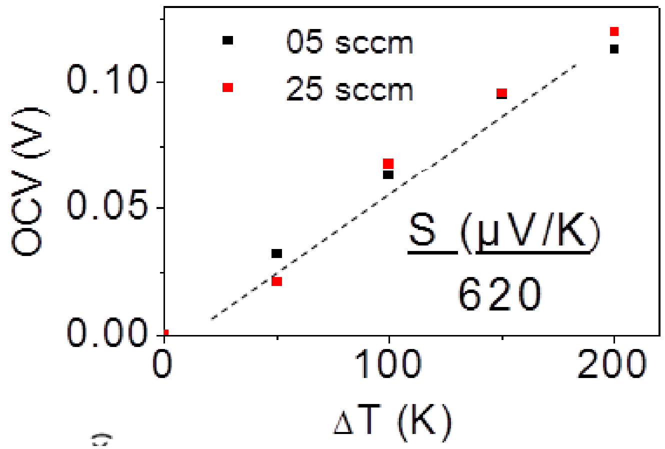
520 ºC **630 ºC** **725 ºC**

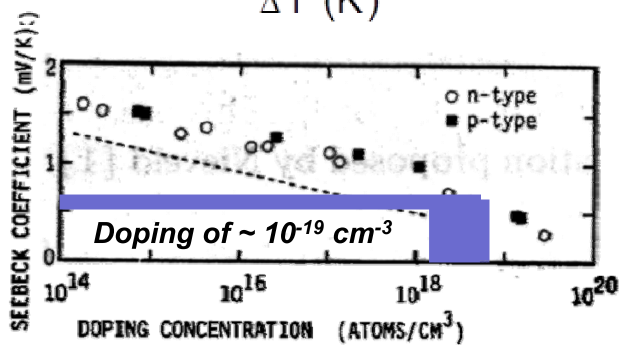


From G. Gadea et al., ***Nanotechnology***, *26 (2015) 195302*

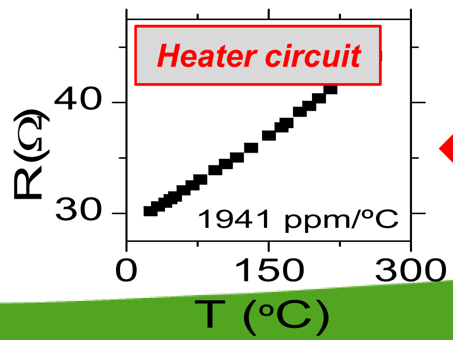
Integration in devices and effect of diborane flow

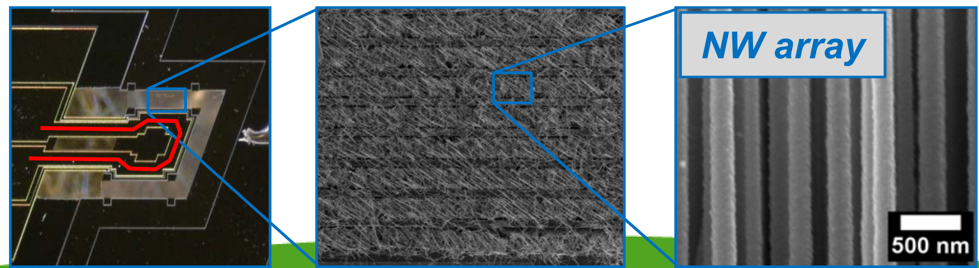






*From A. Van Herwaarden, **Sensors and Actuators** 6 (1984) 245.*





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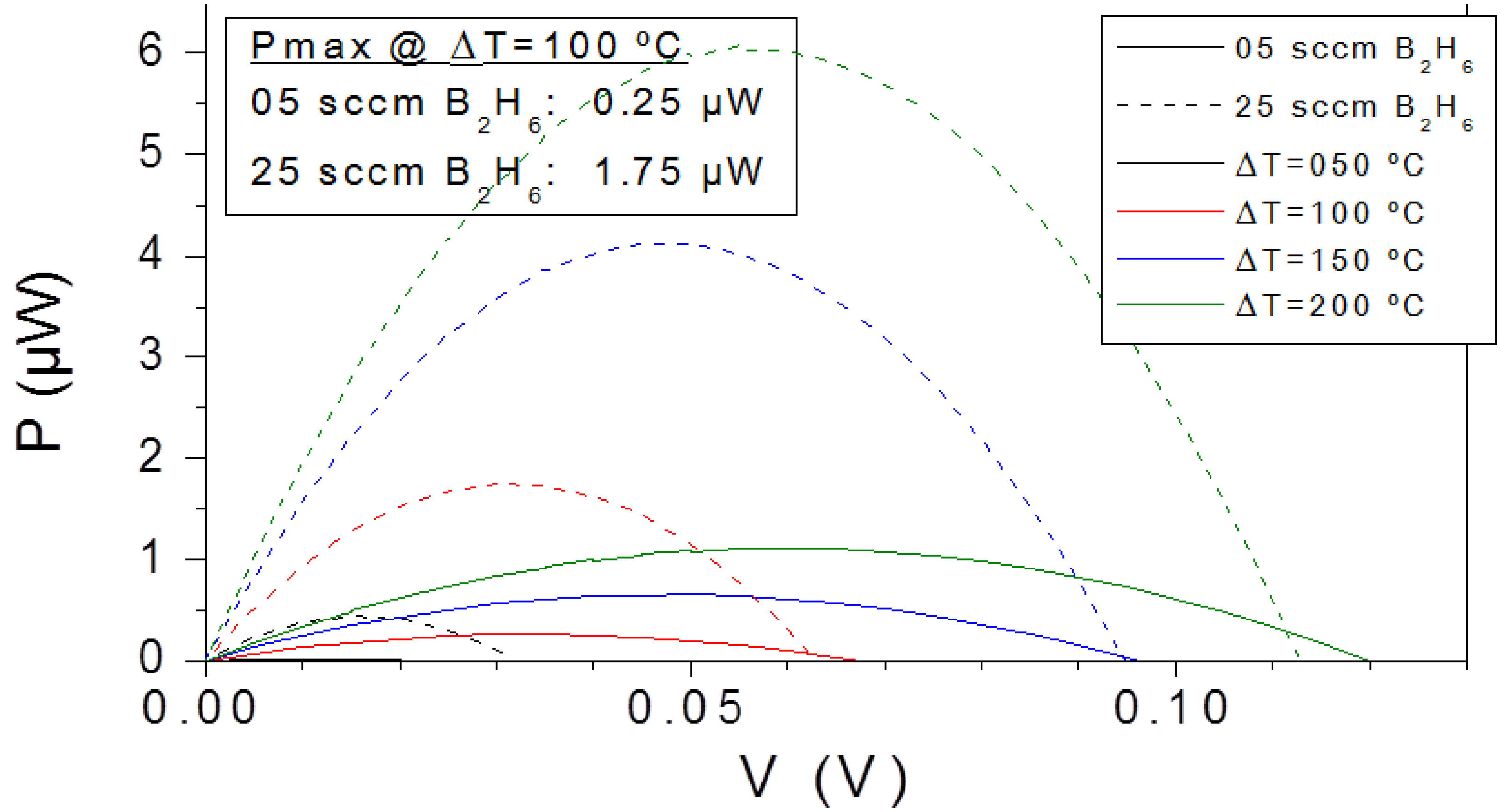
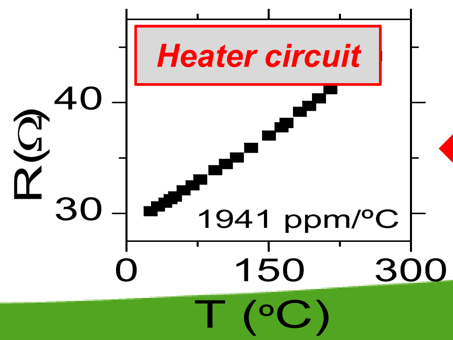
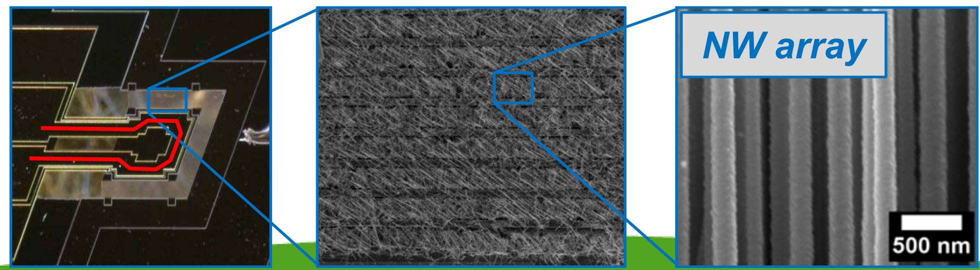
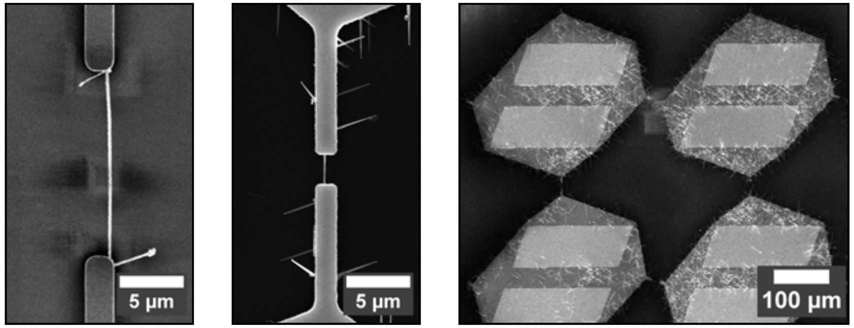
Integration in devices and effect of diborane flow

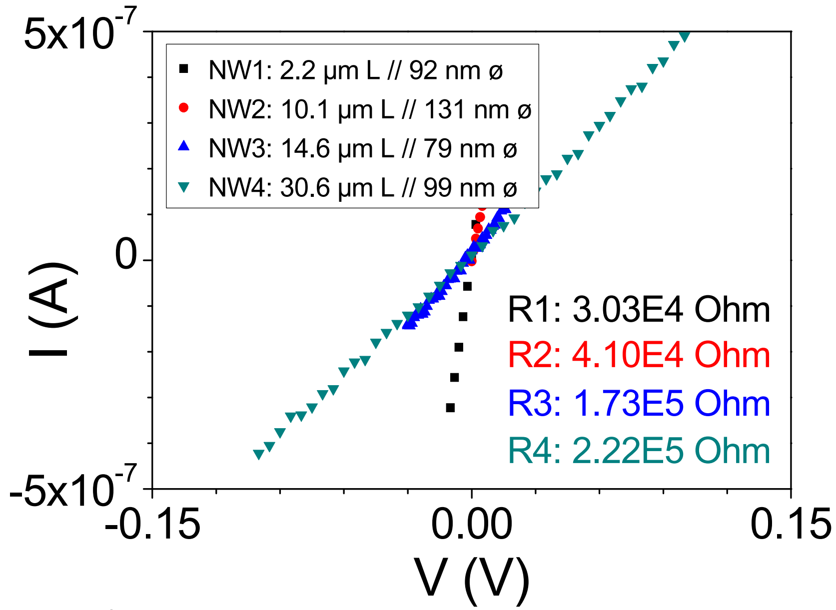


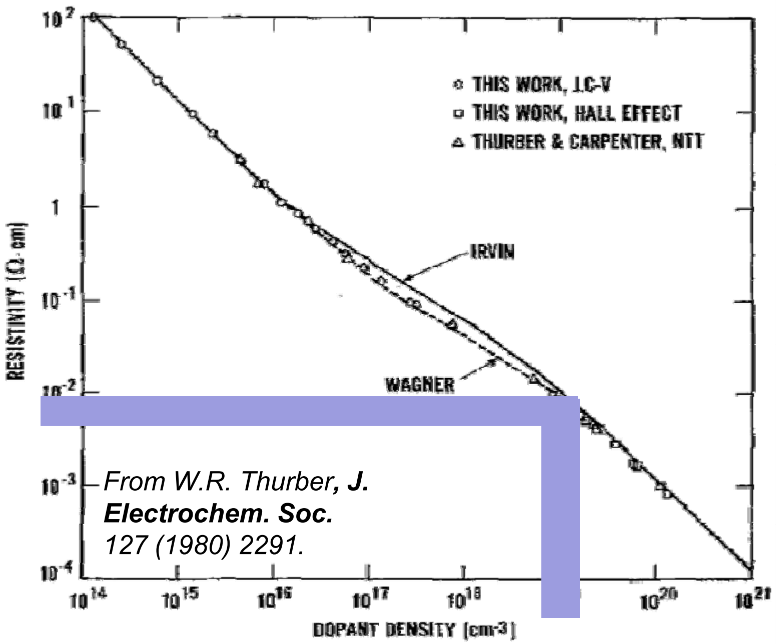


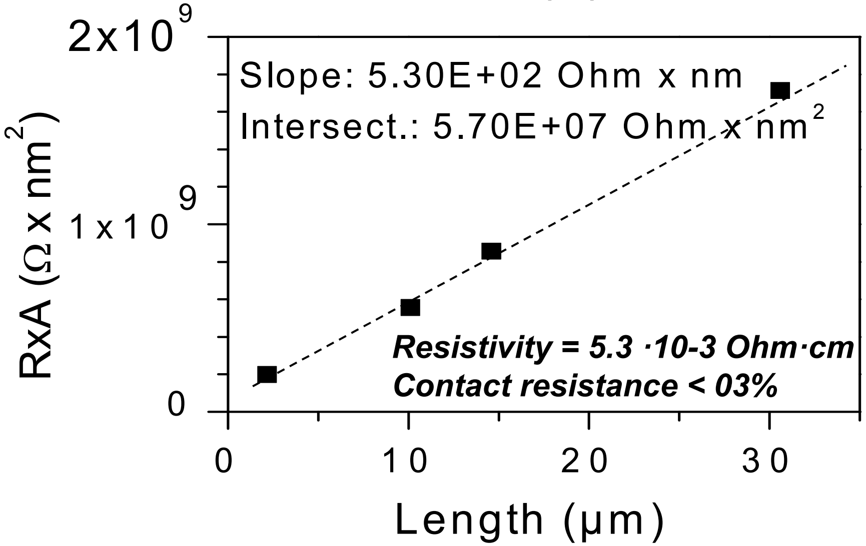


Single NW electrical measurements









Doping of ~ 10^{-19} cm^{-3}

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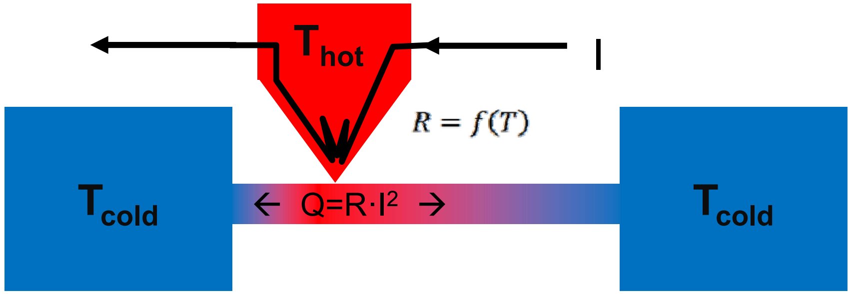
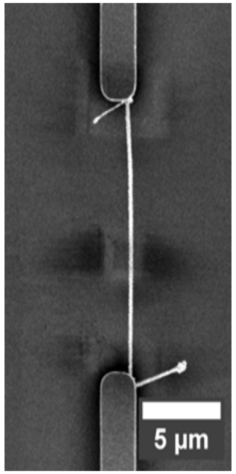
Single NW thermal AFM measurements

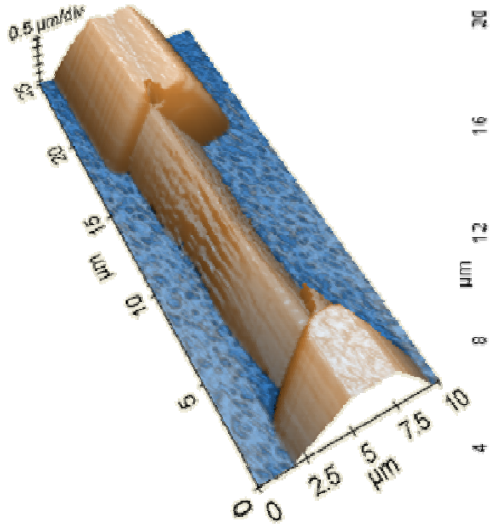


- The thermal afm tip can inject a known heat Q and measure T locally under the tip

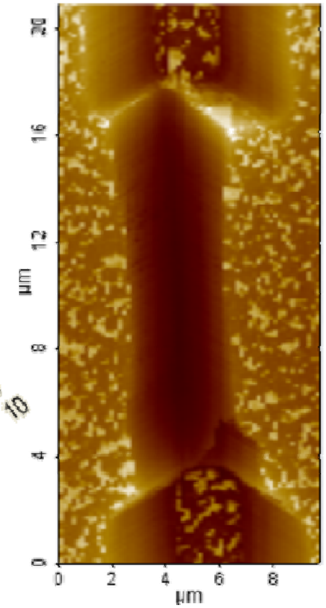
SEM image



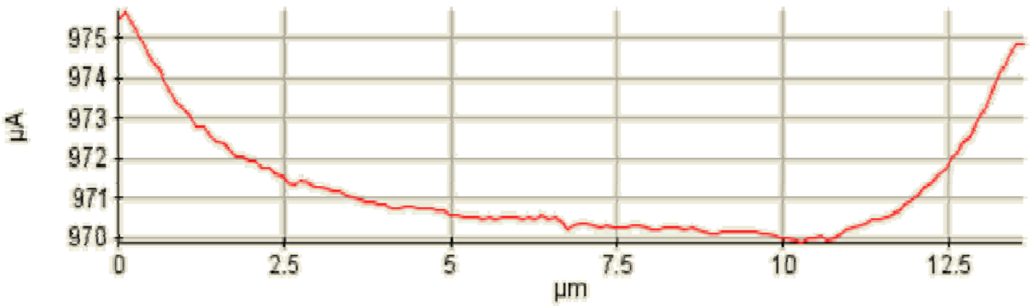
Contact AFM Topography



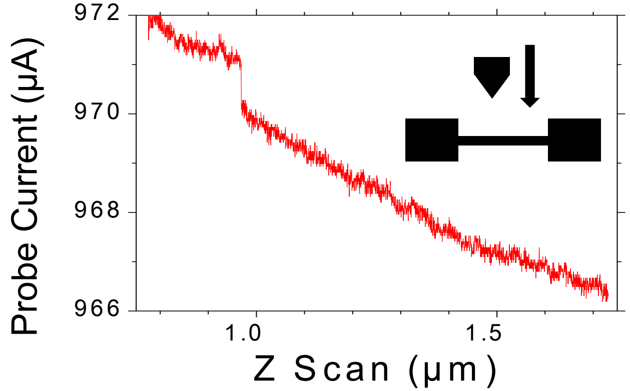
Thermal AFM image



Line scan along the NW



Approach curve



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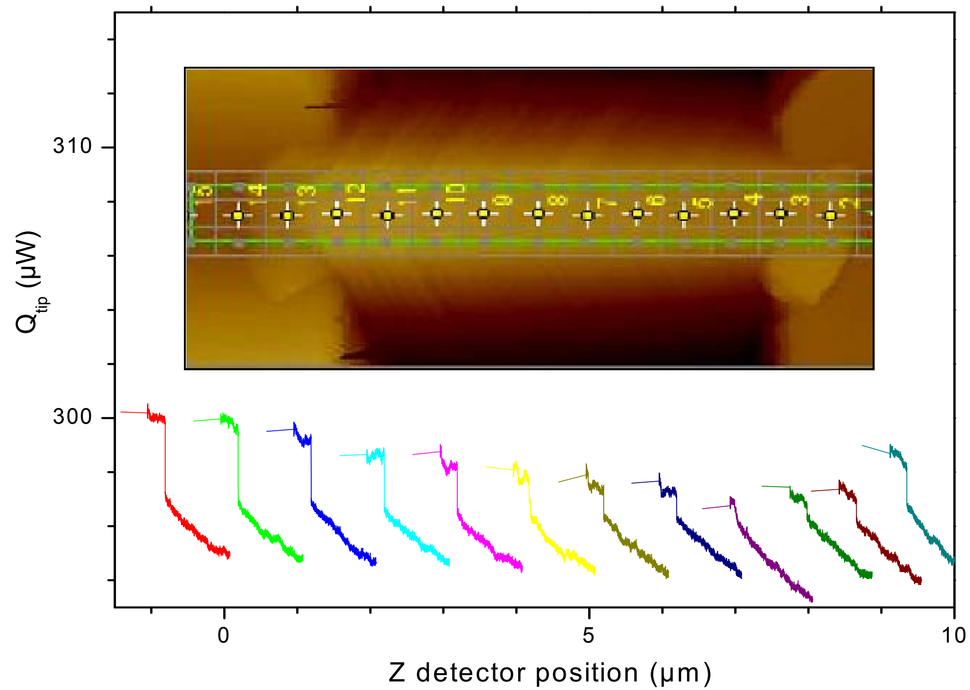
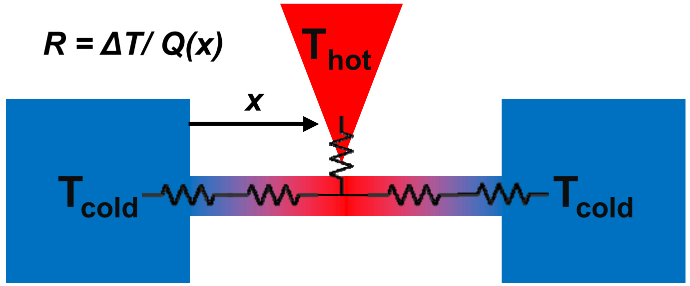
Single NW thermal AFM measurements



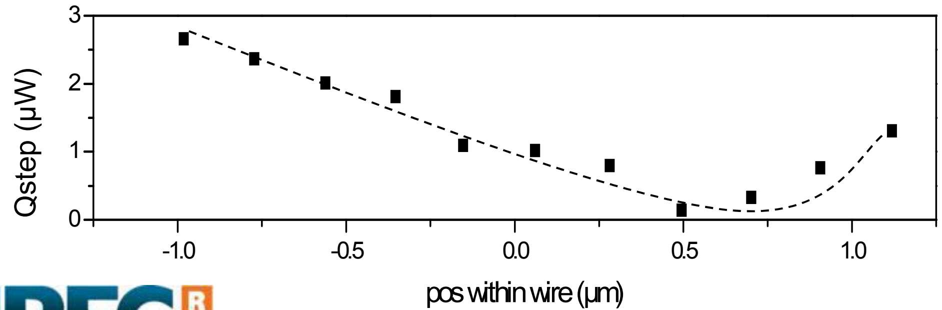


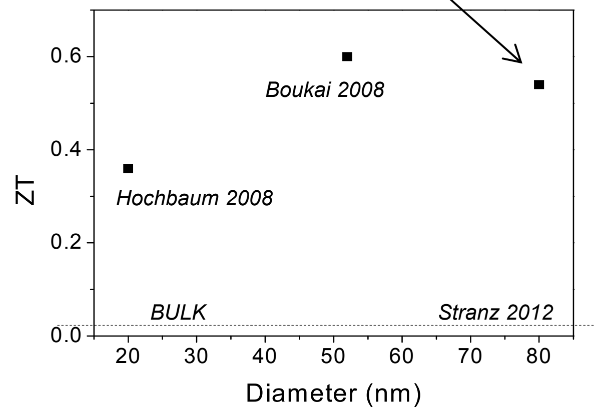
$$R = R_C + \frac{R_{NW}^2 \cdot f(x) + R_S \cdot R_{NW} + R_S^2}{R_{NW} + 2R_S}$$

$$R_{NW} = \frac{L}{A \cdot k_{NW}} \Rightarrow k_{NW} = 4\ W/m \cdot K$$

S = 620 μV/K ***σ = 190 Ω/cm***

ZT @ RT = 0.54





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A. Hochbaum et al. Enhanced thermoelectric performance of rough silicon nanowires. ***Nature****, 451(7175), 163–7*

A. Boukai et al. Silicon nanowires as efficient thermoelectric materials. ***Nature****, 451(2008) 7175*

Stranz et al. Thermoelectric Properties of High-Doped Silicon from Room Temperature to 900 K. ***Journal of Electronic Materials****, 42(7) (2012), 2381–2387.*

Conclusions

- 111 Si NWs were grown. Their properties could be controlled through:
  - Au catalyst deposition (selective deposition, density and size)
  - CVD growth (length, doping)
- Si NWs arrays were integrated in thermoelectric microgenerators and characterized
  - Seebeck coefficient was 620 μV/K
  - Higher dopant flow leaded to higher power (25 $\mu W/cm^2$)
- Single Si NWs were integrated in thermoelectric characterization structures
  - Electrical resistivity was $5.3 \cdot 10^{-3}$ Ω·cm and negligible electrical contact resistance
  - Thermal conductivity was 4 W/m·K by, by means of **thermal AFM along a single wire**
- Combining the results a ZT of 0.54 at room temperature was obtained. ~ 25 times higher than bulk silicon value

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Acknowledgements

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- D. Dávila
- L. Fonseca
- A. Tarancón

And to IRECs NI-SOFC group

IREC Institut de Recerca en Energia de Catalunya Catalonia Institute for Energy Research

CNM Centro Nacional de Microelectrónica IMB

SiNERGY

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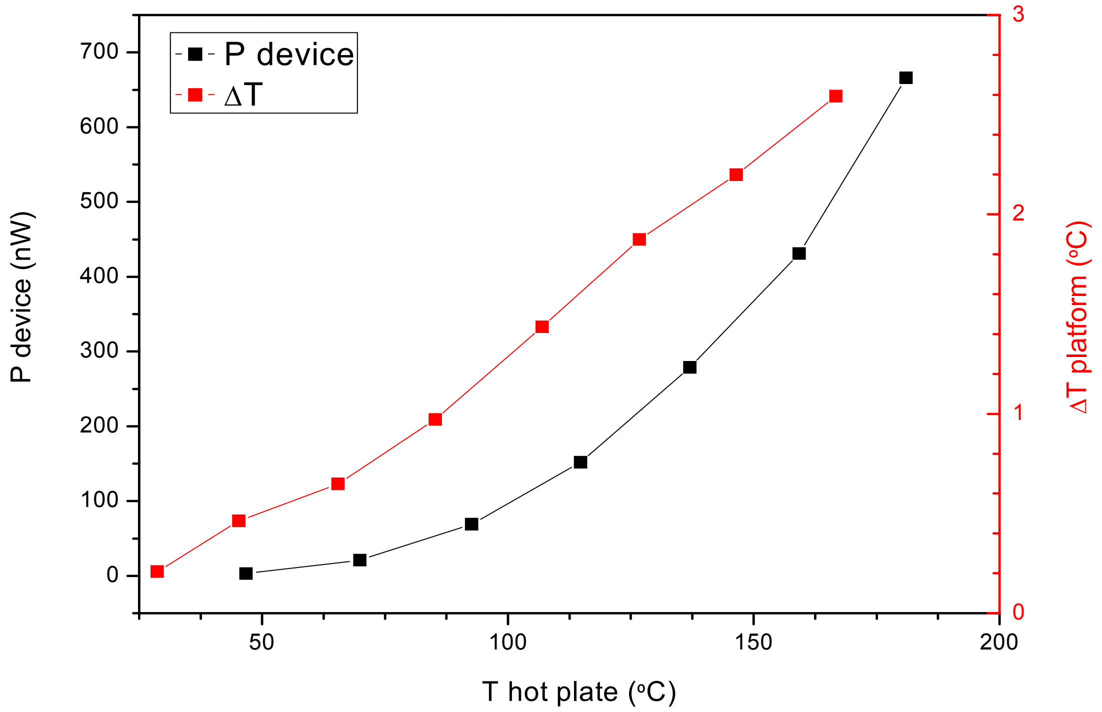
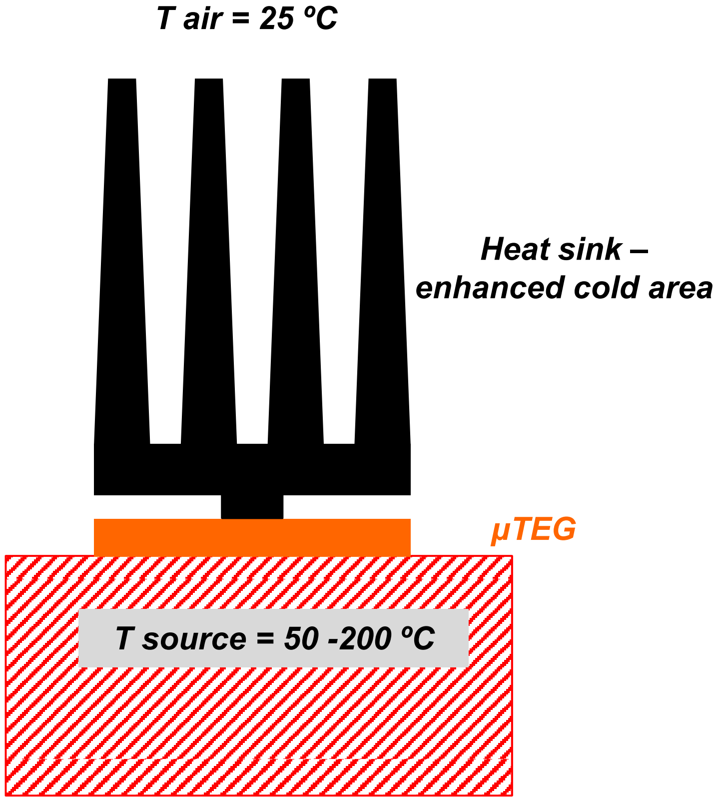
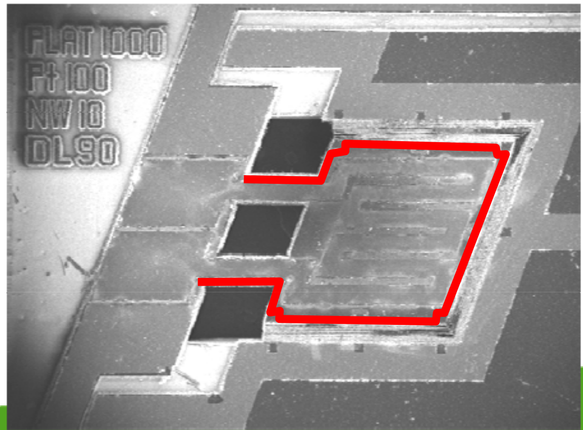
Device in harvesting mode







1 NW/μm2 ***5·10^{-3} Ohm·cm***

R expected *NW array = 1 Ω*

R measured *NW array 50-100 Ω*

R collector *path = 200 Ω*

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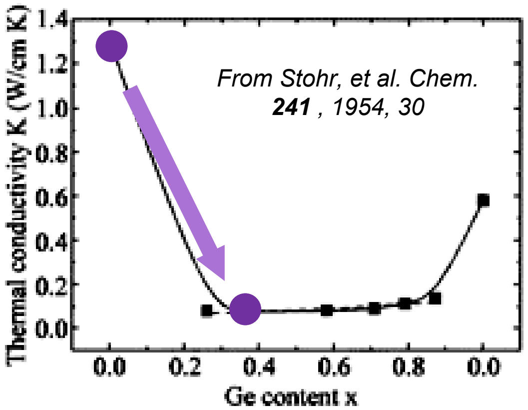
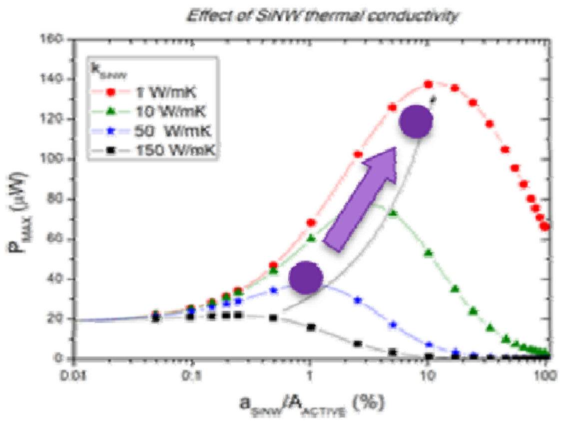
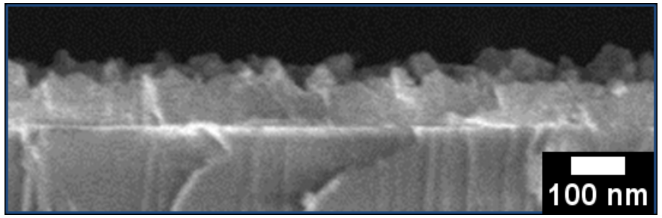
Growth of Si-Ge NWs for future integration in µTEG



Si-Ge allowing should lead to a drastic reduction in NW thermal conductivity

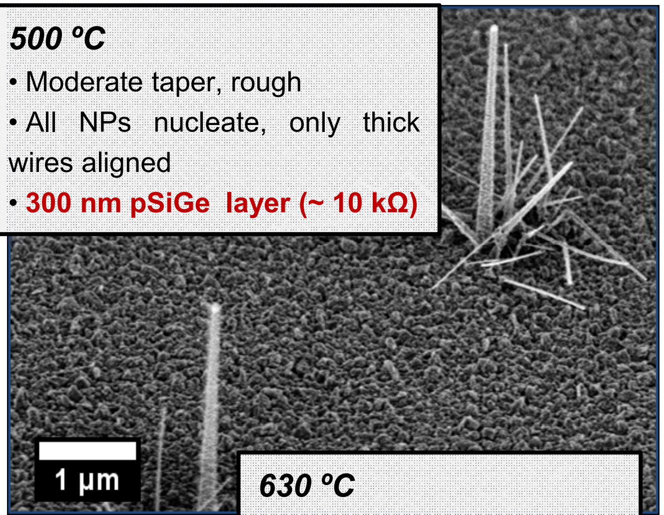


Implementation in devices is expected to increase the power by a factor of 5-10



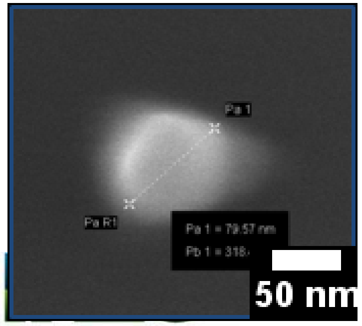
_500 ºC_

- Moderate taper, rough
- All NPs nucleate, only thick wires aligned
- **300 nm pSiGe layer (~ 10 kΩ)**



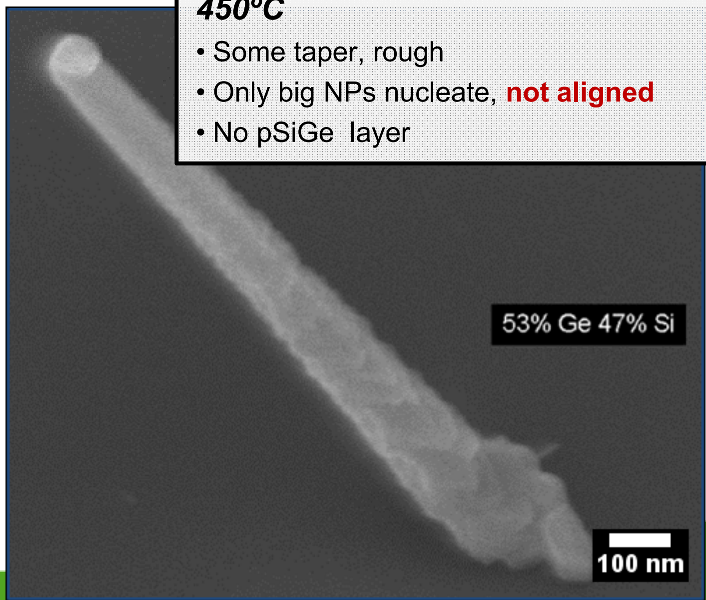
_400 ºC_

- No nucleation at all
- No pSiGe layer



_450ºC_

- Some taper, rough
- Only big NPs nucleate, **not aligned**
- No pSiGe layer



_630 ºC_

- Rough, tapered
- All NPs nucleate, ~ aligned
- **> 500 nm pSiGe layer**