SiNERGY

E·MRS 2016 Spring Meeting

Integration path for an all-silicon MEMS based thermoelectric micro and nanogenerator

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Outline

- Introduction
- Thermoelectric microgenerator conception
- Silicon microplatform fabrication
- Nanostructured active material integration
- Interface with the environment
- Conclusions and further work

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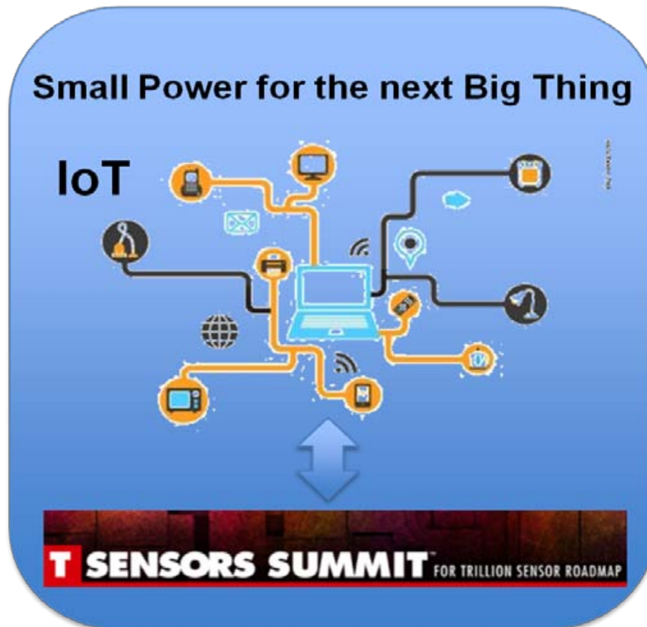
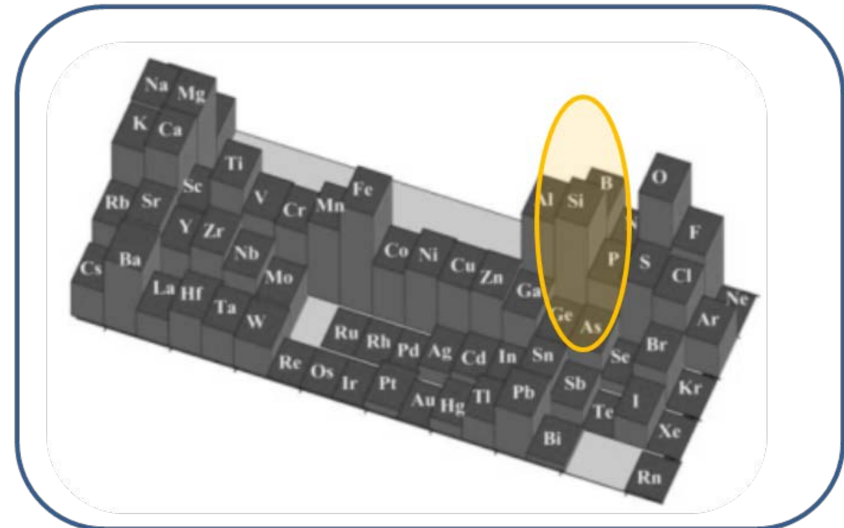
Introduction

Energy autonomy



Get the energy, or replenish the battery, from the environment

All-silicon implementation



Enabling aspects of Silicon technology

- Abundant material
- Mature fabrication technology
- Cost effectiveness and economy of scale
- Miniaturized systems and dense architectures

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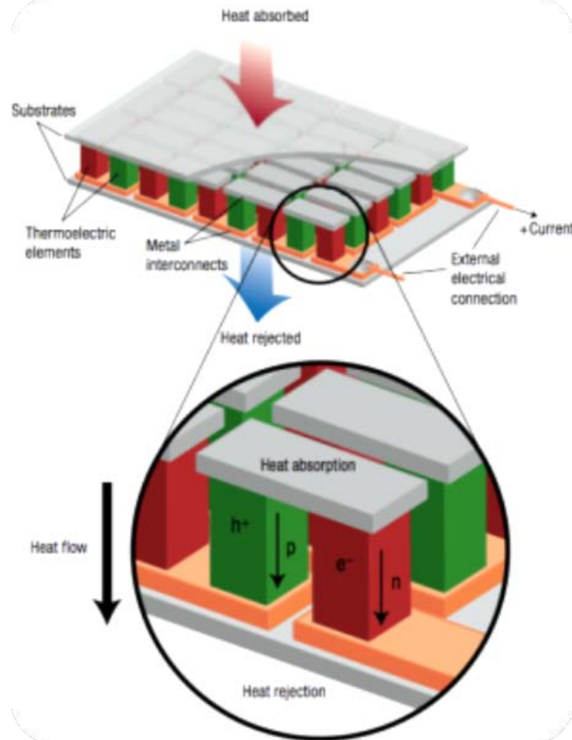
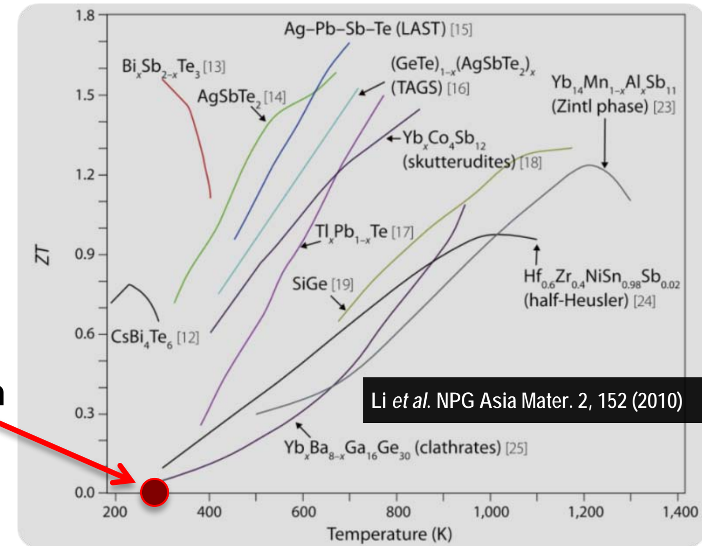
Introduction



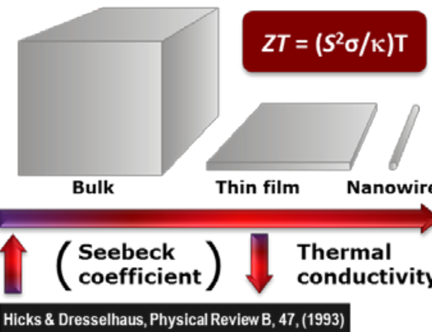
Snyder and Toberer Nature Mater. 7, 105 (2008)

$$ZT = (S^2\sigma/\kappa)T$$

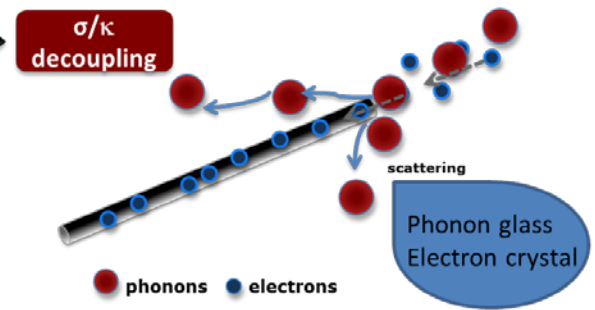
Good thermoelectric material → *ZT* >1



Bulk silicon (ZT≈0.01)



$ZT = (S^2\sigma/\kappa)T$ → σ/κ decoupling



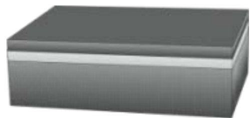
Hicks & Dresselhaus, Physical Review B, 47, (1993)

SINGLE SILICON NANOWIRES with $ZT \approx 1$ → (2008)

Thermoelectric microgenerator conception

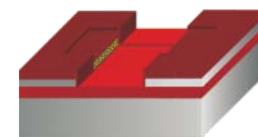
- Large number of Si NWs
- Electrically connected with low R

<110> SOI starting wafer

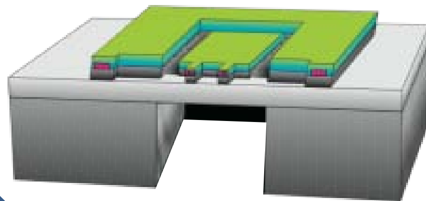


Growth of horizontal Si NWs arrays clamping pre-defined Si structures

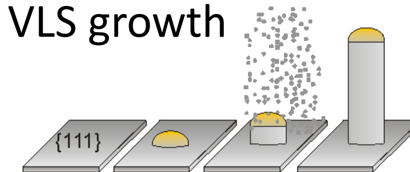
Galvanic displacement

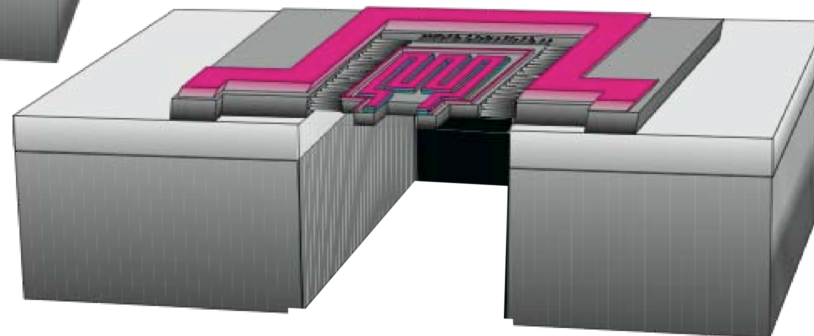


<111> Vertical trenches



VLS growth





Top-down Si micromachining

Bottom-up Si NW growth

Trench depth: 15 µm
Si NWs length: 10 µm
Si NWs diameter: 50-100 nm

MONOLITHIC

PLANAR

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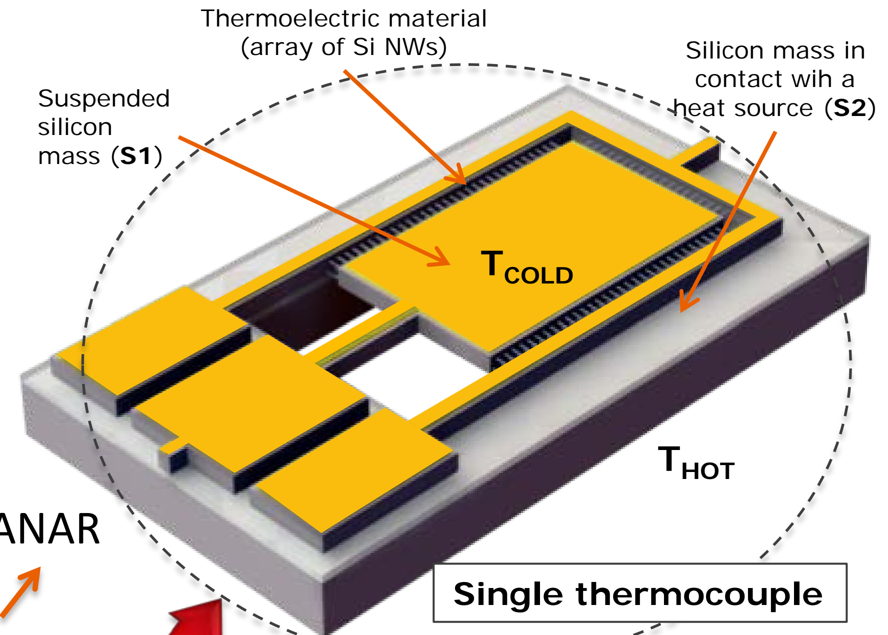
Thermoelectric microgenerator conception

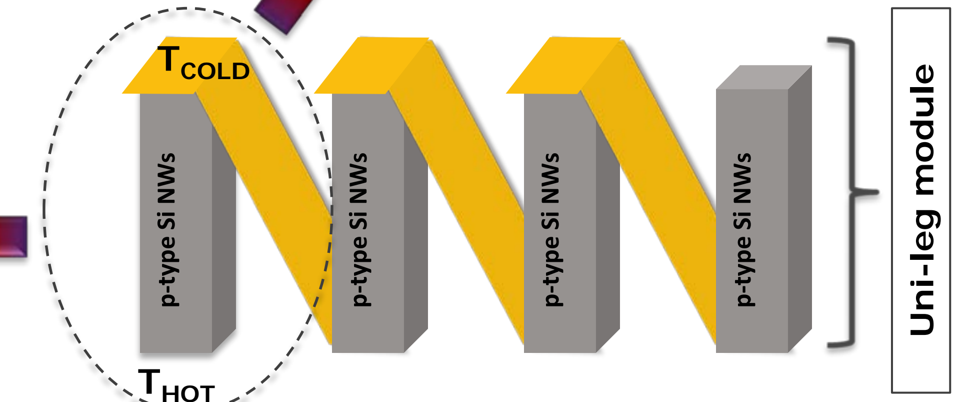
Unique features:

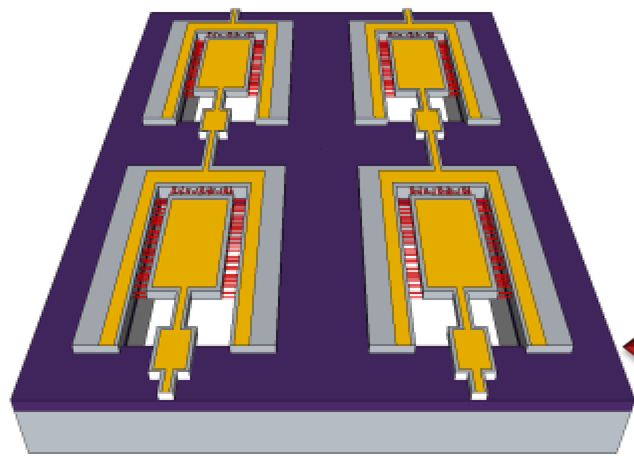
- **Uni-leg** architecture
- Material → (**all**) **silicon**
- **"3D"** SiNWs arrangement **(10^6)**
- **Planar architecture**
- Scalability → series and/or parallel connections



PLANAR

VERTICAL





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Silicon microplatform fabrication

<110> SOI wafer *p*-doped:
15 µm Si device layer
1 µm BOX layer

Si | SiO_2 | LPCVD Si_3N_4 | Metal | Passivation | Al | Si NWs

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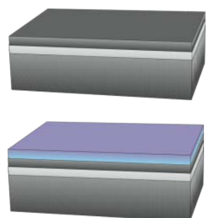
Silicon microplatform fabrication



Si_3N_4 deposition: Membrane support for metal lines & electrical isolation of test structures

Si | SiO_2 | LPCVD Si_3N_4 | Metal | Passivation | Al | Si NWs

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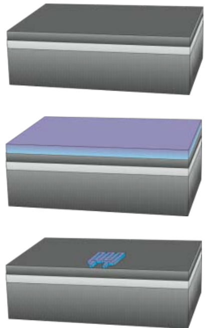
Silicon microplatform fabrication



Patterning of the Nitride layer to open contact regions
Local shallow B implantation for contact formation

Si | SiO_2 | LPCVD Si_3N_4 | Metal | Passivation | Al | Si NWs

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Silicon microplatform fabrication

Metal deposition (W) + lift-off.
Thermal treatment to improve Si/W contacts.

Si | SiO_2 | LPCVD Si_3N_4 | Metal | Passivation | Al | Si NWs

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Silicon microplatform fabrication

Passivation layer deposition:
Avoids metal exposure during NW growth
Partially etched in contact pads

Si | SiO_2 | LPCVD Si_3N_4 | Metal | Passivation | Al | Si NWs

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Silicon microplatform fabrication

DRIE of Passivation, Si_3N_4 and Si device layer:
Main device structure, to be completed with Si NWs

Si | SiO_2 | LPCVD Si_3N_4 | Metal | Passivation | Al | Si NWs

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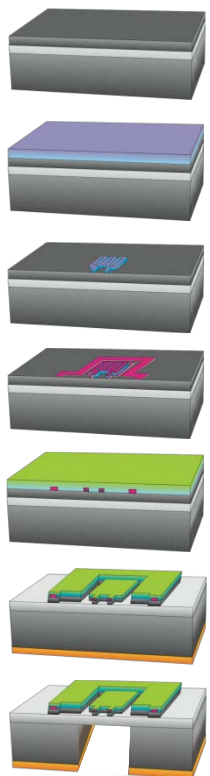
Silicon microplatform fabrication



DRIE of the handle wafer:
Thermal isolation of device regions

Si | SiO_2 | LPCVD Si_3N_4 | Metal | Passivation | Al | Si NWs

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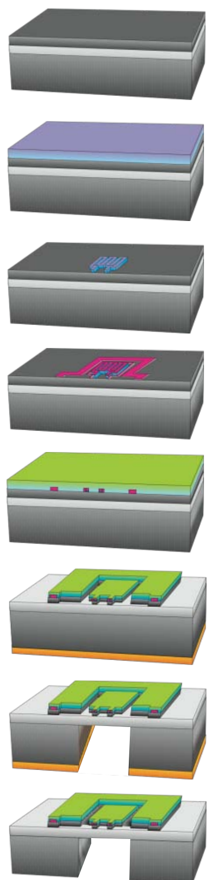
Silicon microplatform fabrication



Al layer removal + Wafer cut
KOH membrane release + BOX removal
NWs growth

Si | SiO_2 | LPCVD Si_3N_4 | Metal | Passivation | Al | Si NWs

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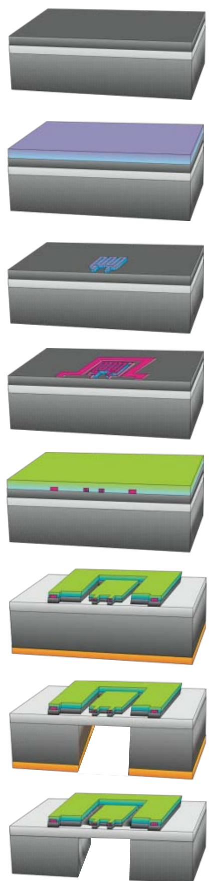
Silicon microplatform fabrication



- Si NWs lenght: 10 μm
- Si NWs diameter: 50-100 nm

Si | SiO_2 | LPCVD Si_3N_4 | Metal | Passivation | Al | Si NWs

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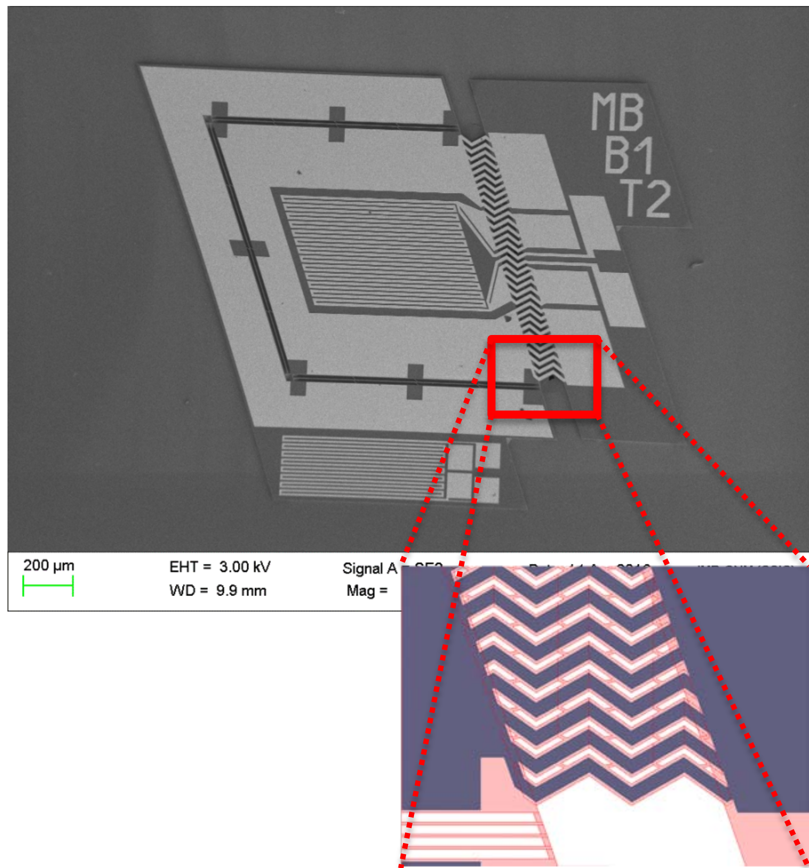
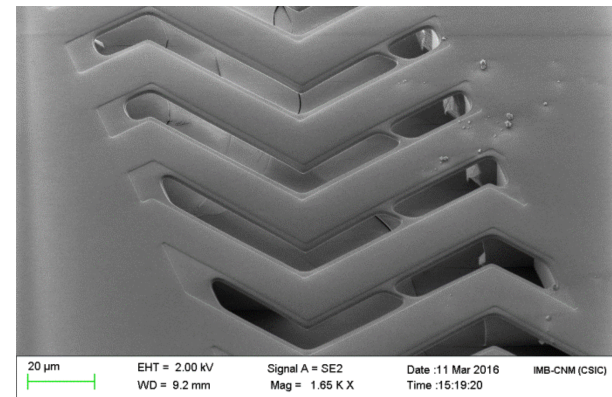
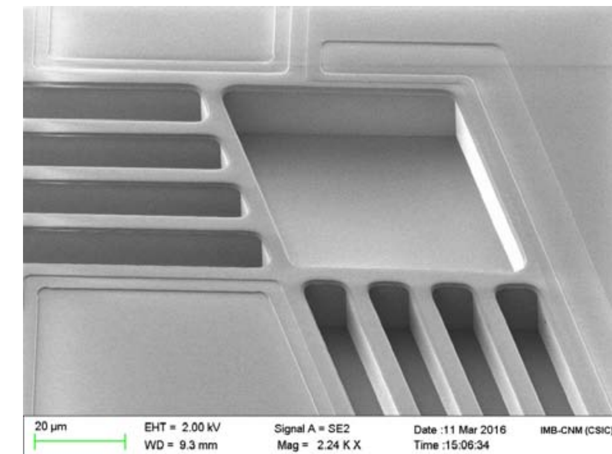
Silicon microplatform fabrication

- Membrane is released with short KOH etch preserving <111> structures.
- Reduces internal resistance and allows arbitrarily long membranes.







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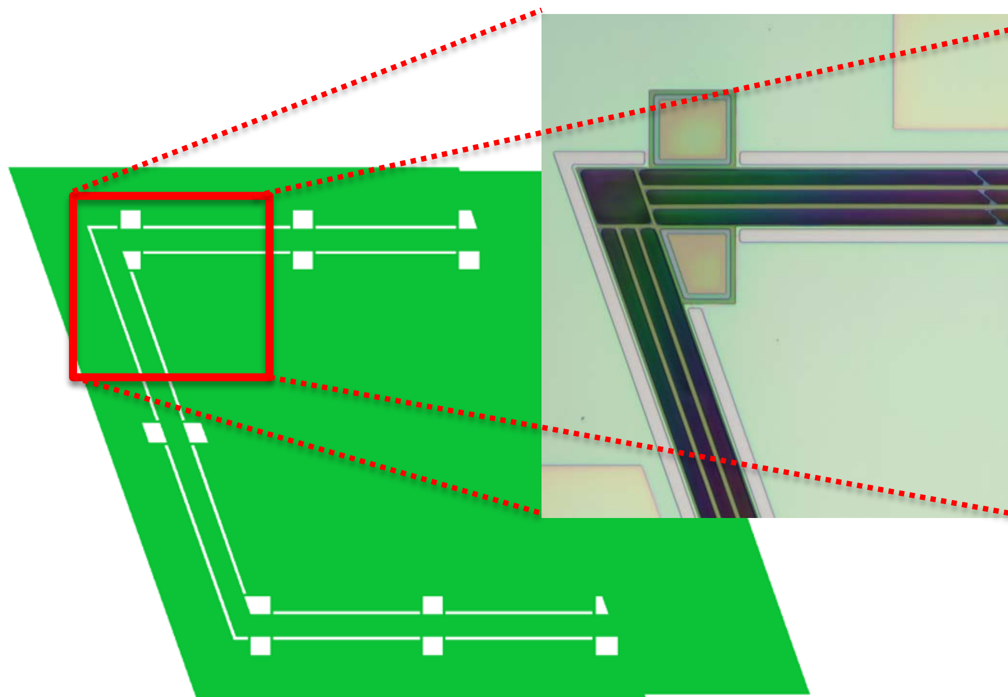
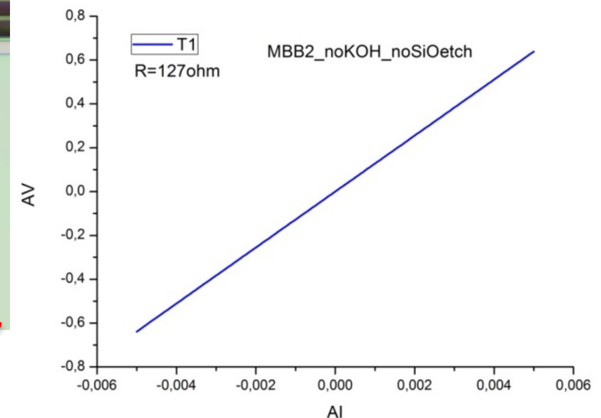
Silicon microplatform fabrication

- Local B implantation (5E15 at/cm^2 and 50 keV) using nitride layer as a mask and thermal treatment (RTA @ >600ºC in vacuum) provide ohmic contacts.

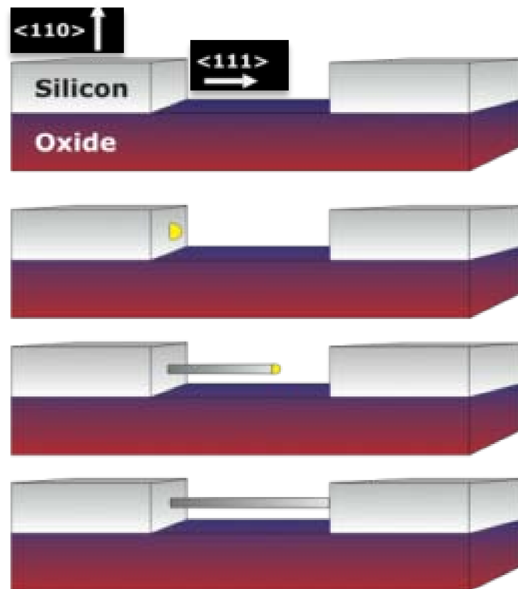




Nanostructured active material integration

Horizontal growth of Si nanowires

- **Galvanic displacement**
  - Selective deposition of Au nanoparticles only on Si surfaces.
  - Control of nanoparticle size and density.
- **VLS growth method** (quasi-epitaxial)



SiH_4

Under 700°C

(Ø 80-100 nm)

Dense & homogeneous multiple linked arrays of Si NWs

❖**Mechanically robust**
❖**Electrically continuous**

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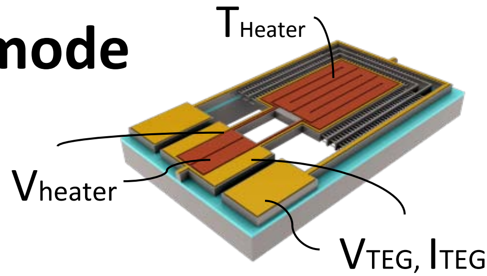
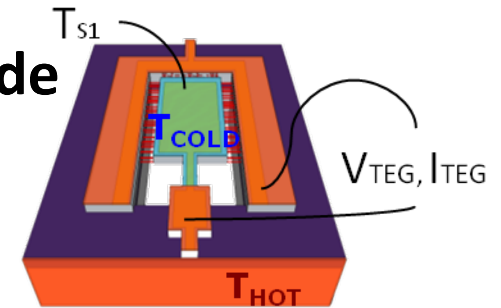
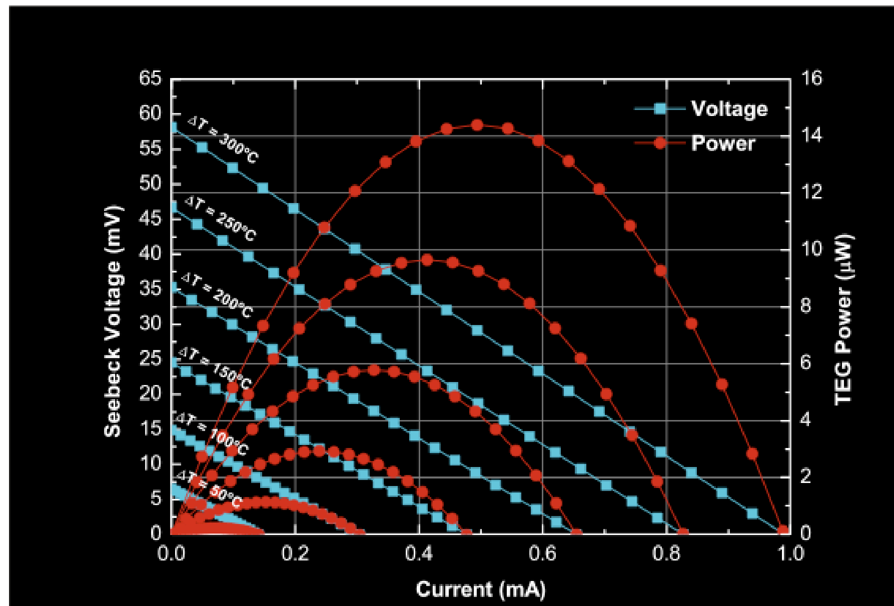
Nanostructured active material integration

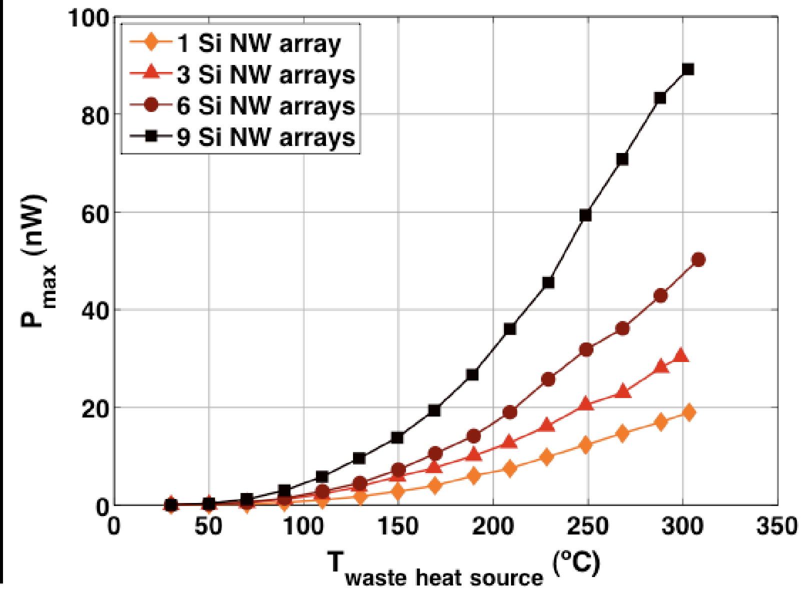
Test mode



Harvesting mode







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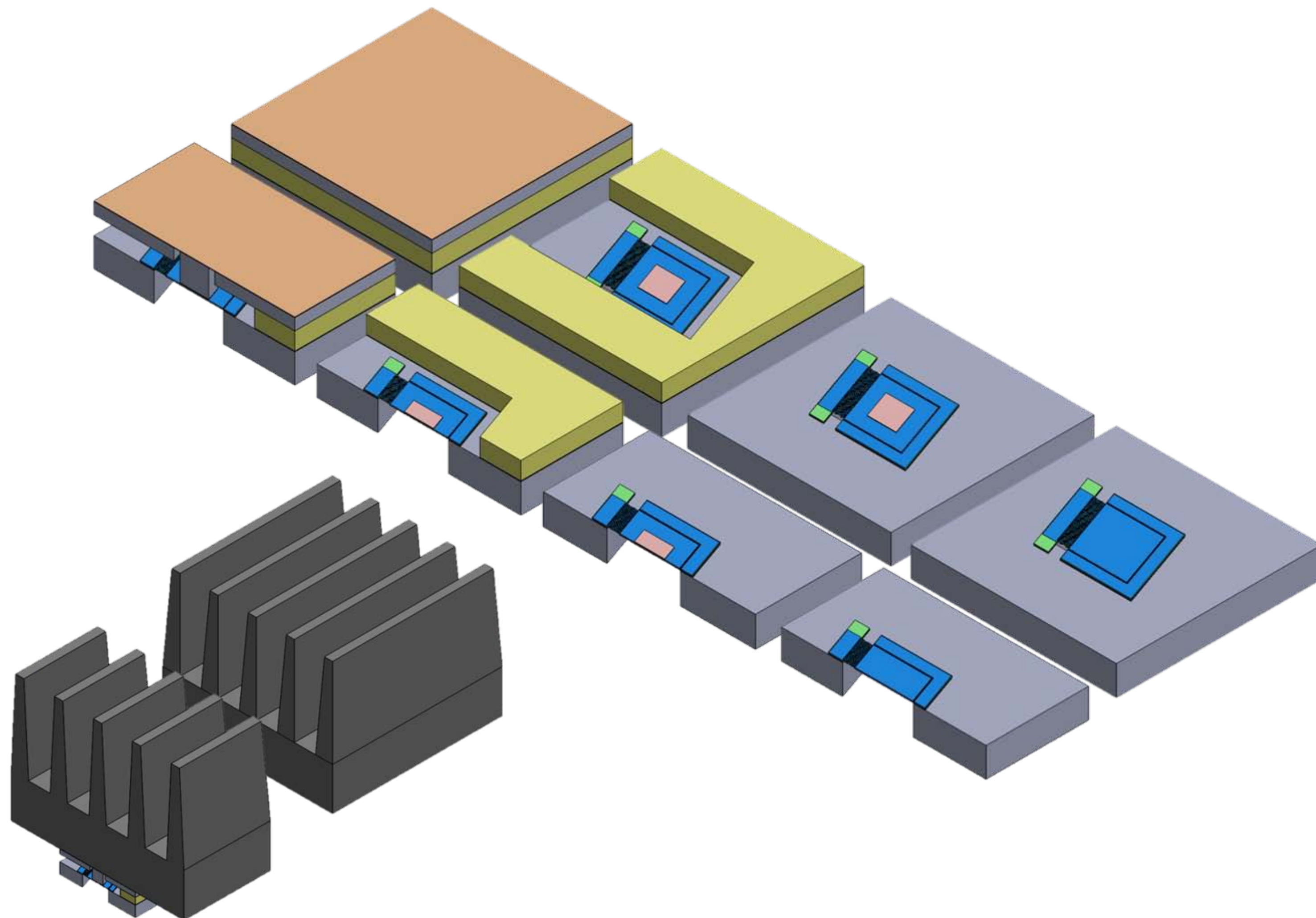
Interface with the environment



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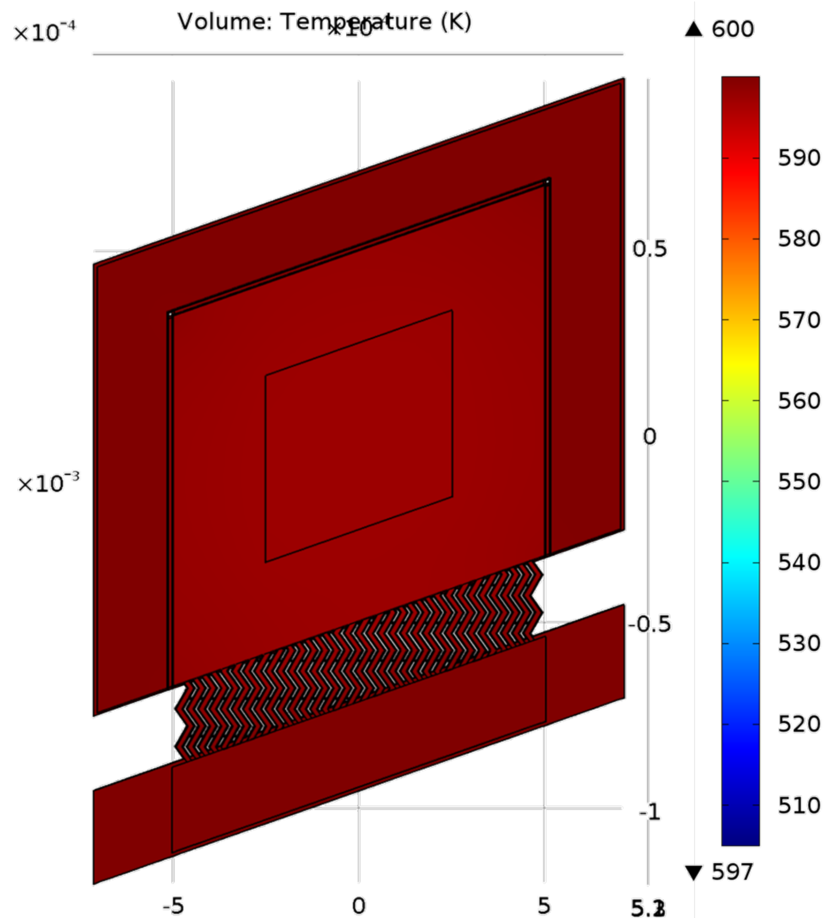

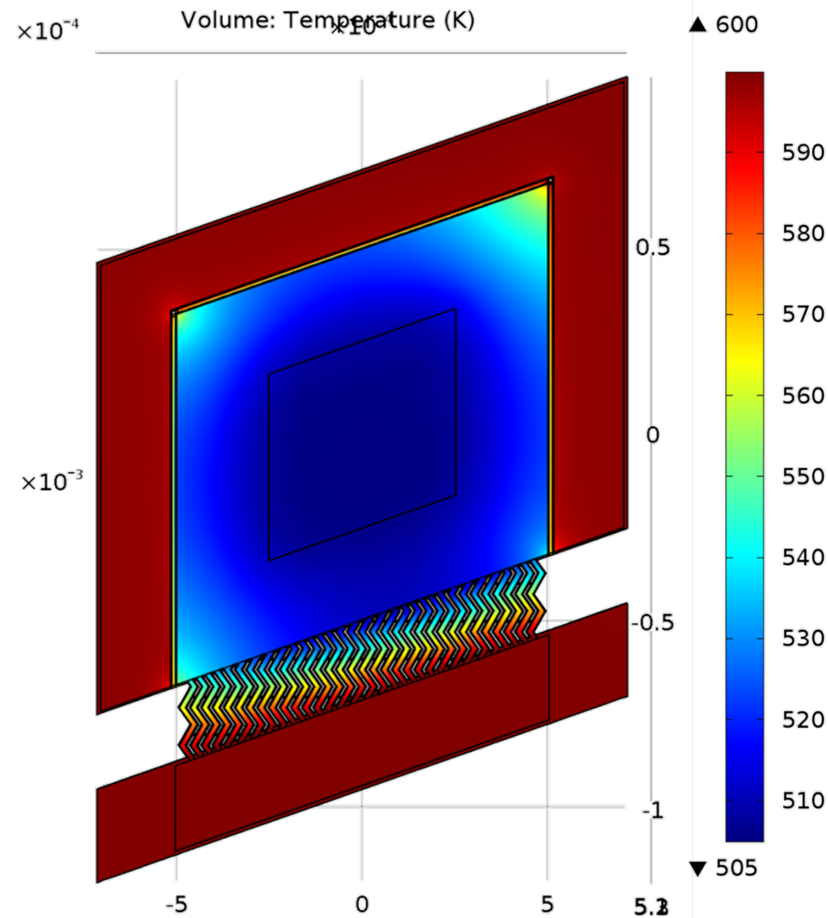

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Conclusions and further work

- A route to fabricate all-Si thermoelectric microgenerators using arrays of Si NWs as active material has been settled.

- Microplatforms with optimized thermal isolation (low-k supports), Si NWs arrays of arbitrary length (Si spacers) and improved Si/W contact resistance have been produced.

- The integration of Si NWs in such structures and the operation as thermoelectric generators has been demonstrated.

- Progress needed to integrate a dissipator with these platforms in order to favor the heat flow through the active material and increase the Δt across the NWs.

- Design of new optimized architectures (power per unit area).

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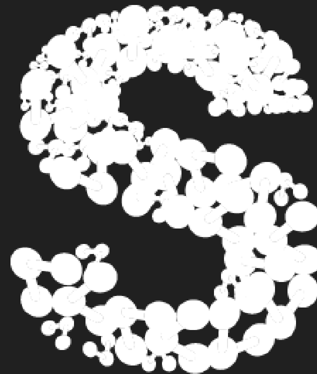
Thanks for your attention!



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